

APPLICATION NOTE

TDA8752
Demonstration board documentation

AN 97022



APPLICATION NOTE

Triple high speed analog to digital converter for LCD drive.- TDA8752

AN/97022

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Keywords

Demonstration board
8 bit, high speed data conversion
Triple ADC for LCD drive
PLL, AGC control, CLAMP control on chip

Date : March 1997

Summary

This note describes the demonstration board (n°534 or 514) done for the evaluation of the TDA8752, triple 8 bits analog to digital converter.

It describes as well how to use the TDA8752 with a LCD screen, quite easily, how to program the TDA8752 registers either by using the I²C software or with the help of the interface board (PCB n°453). A short description of the I²C software takes place in this report, and also how to use the interface board and the associated software.

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1. INTRODUCTION

The TDA8752 is a triple 8 bits high speed analog to digital converter. It has been designed for R, G, B high speed digitizing, for LCD panels drive, for LCD projection systems and video systems. It can be used for VGA or higher resolutions LCD panels, such as the one described in annex 5 (up to 80MHz using just one TDA8752, and up to 160MHz pixel frequency using two chips in parallel).

There are on chip a PLL, an AGC, a clamp system. All these functions are controlled by the programming of registers with the help of I²C or 3 wire bus communications. The main characteristics of this converter are the following:

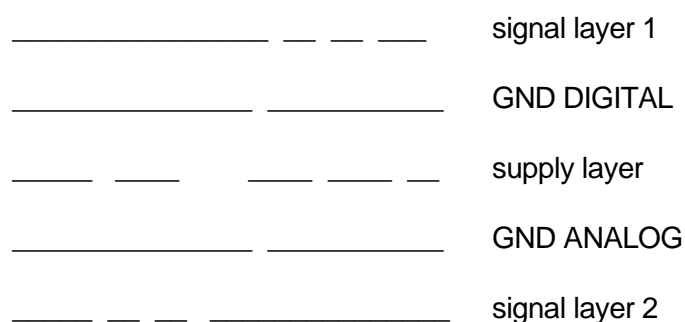
- According to the gain range (using fine and coarse gain registers), the input signal is from 0.4V to 1.2V to be able to produce full scale ADC input.
- The clamp level is controlled from the code -63.5 to +64 in steps of ½ LSB.
- The sampling frequency for the ADC is provided by the PLL, which is locked on a line frequency from 15KHz to 280KHz. The outputs CKAOUT and CKBOUT can be independantly phase shifted from 0° to 180° by steps of 11.25°; this is done through registers programming. For a 180° phase shift, the INV pin can be used.
- The typical power dissipation is 1W.

The application board requires some external components to drive the circuit in a system environnement, that is to say VGA input, LCD screen, and to control the TDA8752 registers either an I²C interface board (see §2.2), very easy to use for an I²C communication, or a microcontroller interface board (see § 5.1) for a communication either with I²C bus or 3 wire bus. The communication type choice is done by hardware on the chip either via a switch, when the I²C interface board is used, or via the multiplexer when the microcontroller board is connected.

The TDA8752 has a wide range of applications. That is why for the demonstration board, all the settings were chosen, at first, to drive a LCD screen of 800×525 (600×480 active pixels), referenced LDH102T-20 from FPD (Flat Panel Display CO, annex 5), with a VGA input signal coming out from a PC.

2. STRUCTURE OF THE "TDA8752 DEMO" BOARD

This board is a five layers board: the first one for the signals, the second one mainly for the digital ground, the third one for the supply voltages, the fourth one mainly for the analog ground, and the fifth one for the signals:



The analog and the digital ground are connected together in one point under the TDA8752. The parameters used for the conception of the board are:

- Substrate:	epoxy glass
- Permittivity:	4.7
- Dielectric thickness between layers :	16 mils
- 50 Ω microstrip lines :	W = 0.027 in
- 75 Ω microstrip lines :	W = 0.014 in
- 90 Ω microstrip lines :	W = 0.010 in

Some precautions were taken for the realization :

- All supply voltages are well decoupled the nearest as possible from the circuit for high frequency and at the start point of the supply line for low frequency. All the supply voltages are generated by the same regulator and then are "star connected".
- All the decoupling capacitors are to be the nearest as possible to the circuit, especially RDEC, BDEC, GDEC to avoid oscillations.
- All the inputs (RIN ,GIN, BIN) and the output buses (R0-R7, G0-G7, B0-B7) are very similar to each other with regards to wire resistivity and capacity.
- All the high frequency wires (like CKEXT, CKAOUT, CKBOUT) are quite well separated from the buses and the low frequency wires (like CP, CZ, etc...).

2.1. INPUTS AND SYNCHRONIZATION

2.1.1. Inputs

A cable has to be plugged from the video output (VGA output) of a PC to the VGA connector J3 of the board. To have the possibility to control the image on a monitor and on the LCD screen, in parallel, a second VGA connector, J2, is on the board. A second cable is then plugged between this VGA connector and the monitor. A buffer cell is done (NPN transistors are used) to protect the monitor from what is coming from the demo board.

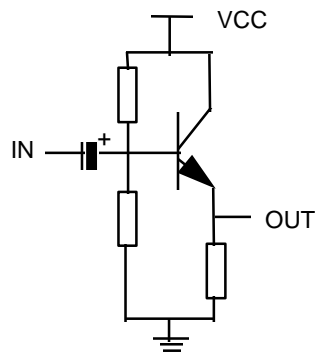


Fig.2 : Buffer cell

The signals, coming from the VGA connection, are the following (Fig.3):

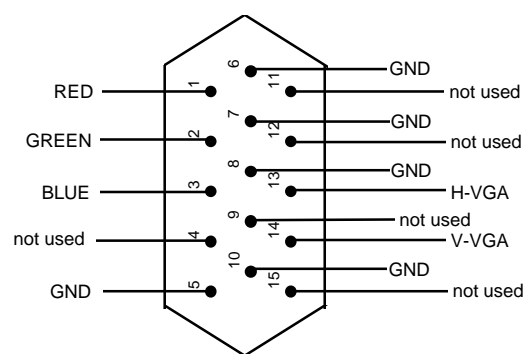


Fig.3 : VGA connector 15 pins

The R, G, B signals are directly connected to the R, G, B, inputs of the TDA8752 converter. The synchronization signals (H-VGA and V-VGA), which are buffered by a resistor connected to the ground in order to avoid jitter, will be used to produce the synchronization signals in order to drive the LCD screen. These signals are named LP and FLM (see the LCD specification in annex n°5).

2.1.2. Synchronization

The method will be the same to generate these two signals, LP and FLM.

- According to the timing diagram of the vertical synchronization, given in annex n°3, the FLM pulse is delayed by 35 lines compared to the VSYNC VGA pulse and its length is 1 line. The principle block diagram is the following (Fig.4):

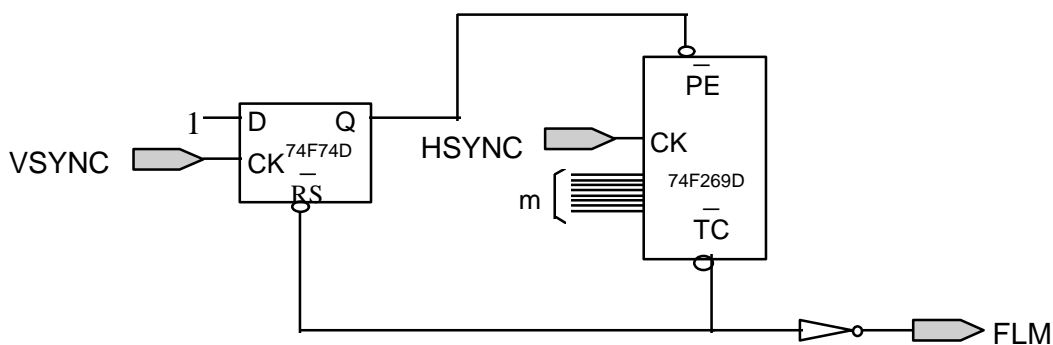


Fig.4 : Principle diagram for the LCD vertical synchronization

The 74F269 is a synchronous 8-stage Up/Down counter. All the state changes are on the rising edge of the clock. The U/D pin permits to choose between the up and down modes: for this application, the counter is in the count down mode. When the PE pin is low, input values are loaded in parallel to the corresponding outputs. The terminal count down is defined with all the outputs at low level. And the TC pin is low if the counter is at the terminal count and if CET is low. As it is described in the following diagram (Fig.5), the counter is set to the programmable value $m = 34$ to respect the timing diagram of the LCD vertical synchronization.

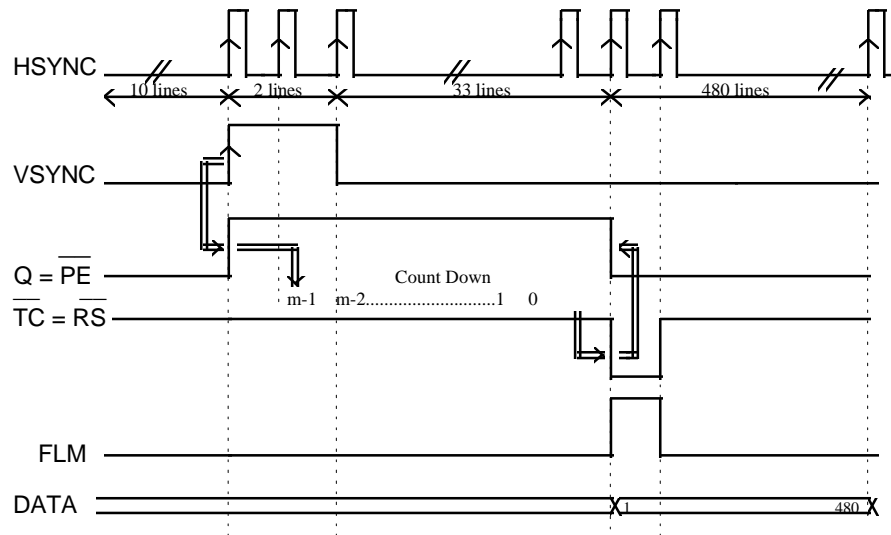


Fig.5 : Generation of the LCD vertical synchronization

The FLM signal is buffered to have no problem of drive capability. The buffer is a 74F125D (IC10).

- The same principle is used to generate the LP signal. The characteristics of this signal are (see annex n°3) :

- * a pulse during n_2 pixels with the relation: $1 < n_2 < 128$
- * a rising edge n_1 pixels after the one of HSYNC (H-VGA)
- * a falling edge 16 pixels before the beginning of the data.

So according to the timing diagrams of the VGA and LCD horizontal synchronization signals, it results in :

$$n_1 + n_2 + 16 = 96 + 48 = 144 \text{ or } n_1 + n_2 = 128$$

Here, it is necessary to have two counters to fix the values n_1 and n_2 . The constants n_1 and n_2 will be defined by switches on the inputs of counters. The block diagram is the following (Fig.6) :

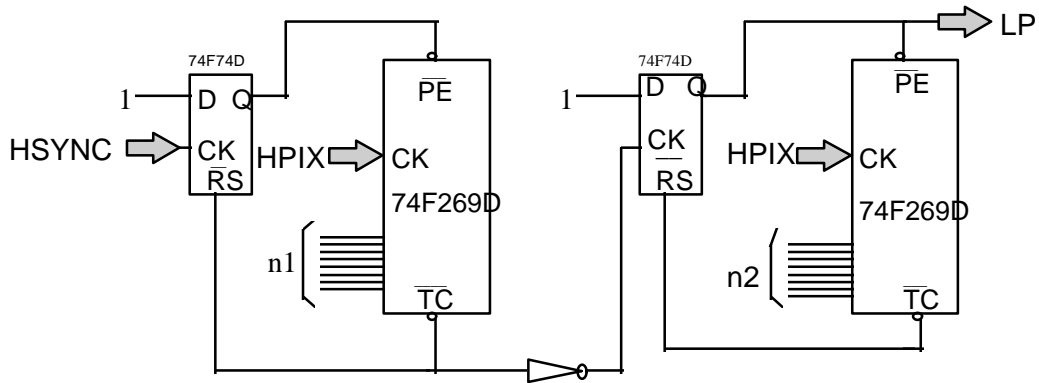


Fig.6 : Principle diagram for the LCD horizontal synchronization

The timing diagram is shown in Fig.7 :

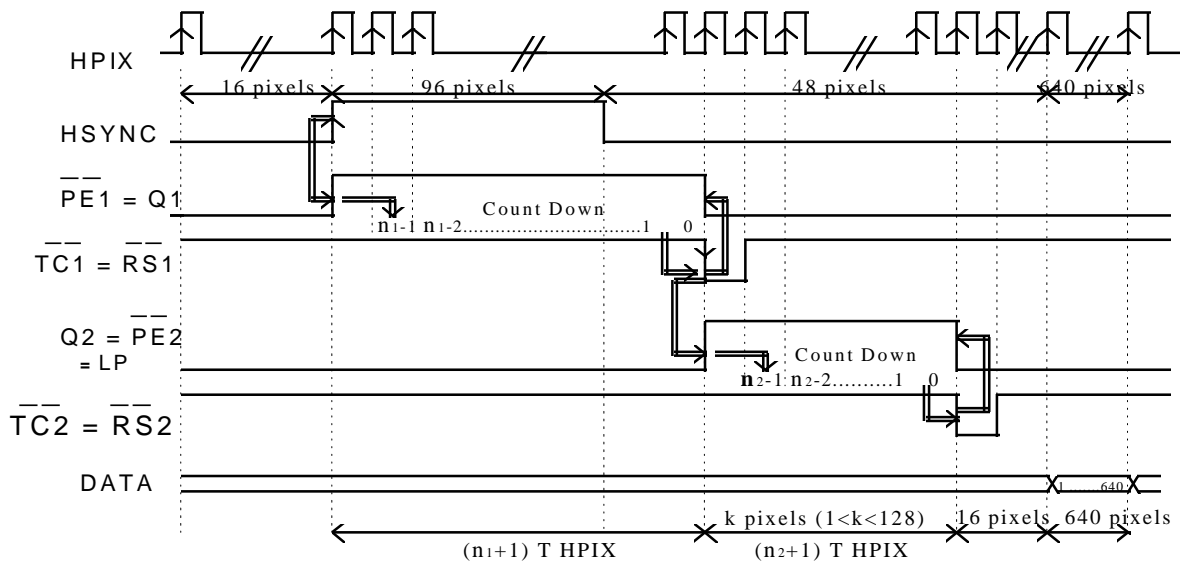


Fig.7 : Generation of the LCD horizontal synchronization

In order to control the signal LP correctly with regards to the pixel clock CKAOUT, CKBOUT (which are the pixel clocks generated by the TDA8752 PLL) will be used, instead of CKAOUT, to control the counter which generates LP.

Then it will be possible to delay independently LP, and to avoid setup and hold timing problem by using one (by closing K27) or two (by closing K30) flip-flops (IC12).

The LP signal is buffered to have no problem of drive capability. The buffer is a 74F125D (IC10), the same as for the FLM signal.

2.2. CONVERSION AND EXTERNAL CONNECTIONS

2.2.1. Conversion

This part concerns more the TDA8752 converter. The R, G, B channels are totally similar. The inputs (xIN) are AC coupled because the polarization voltage is done internally around 2V (Vp voltage). The other pins (xBOT, xGAIN, xDEC) are decoupled to the analog ground to avoid noise and oscillations. The pins xCLP are used to connect a storage capacitance.

To drive the TDA8752, a bus communication must be established either with a 3 wire communication or with a I²C communication. If the microcontroller board is used, the multiplexer 74HCT4053T will set up correctly the SDA, SCL, I2C3W pins according to the chosen communication type :

- when the I²C bus is used, the I2C3W pin is set to 1, the SEN pin is not used, and the I²C protocol is respected for the SDA and SCL signals.
- when the 3 wire bus is chosen, the I2C3W is set to 0 and the pin SEN validates the data. In this case SDA line and SCL line are used as "normal" lines.

If the I²C board is used to drive the TDA8752, the pin I2C3W has to be connected to 1 with a strap between TP13 and TP14 only. To ensure the good polarity on the I2C3W pin, when the microcontroller board drives the chip, a strap should be connected between TP13 and TP12 only.

The disable (DIS) pin is hard connected through a switch (K33) either to VCC (to disable the I²C or 3 wire communication) or to ground (to allow a communication). Most of time, this pin will be used when several TDA8752 are used.

To use the TDA8752 with a I²C communication, the addresses ADD1 and ADD2 must be fixed by the switches K32 and K31. On this demonstration board, the chosen address will be 00.

Concerning the sampling clock for the AD converter, either an external clock (CEXT on J4) or an internal clock generated by the PLL can be used. In this case the input clock is the HSYNC clock (H-VGA), coming from the VGA signals.

On the board, the mode power off is accessible with the switch K28 and the output enable mode as well with the switch K29. Both are active at high level.

2.2.2. Clock system generation

To sample the data, it is possible to use either an external clock or a clock generated internally by the PLL.

When the external clock is selected, the bit Cka from the PHASEA register has to be at 1. The connection is done on J4. In this case, it is not possible to control the sampling moment by using the phase shifter implemented in the chip. The phase shifter A is by passed and the second clock CKBOUT can not be utilized.

The sampling clock can be generated by an internal PLL. The input of the PLL is the horizontal frequency (CKREF). The sampling frequency is, when the Cka bit is at 0: $F_{CKA} = 2N * F_{CKREF}$, with N the programmable divider ratio. All the parameters, which configure the PLL, are fixed by programming the following registers: CONTROL (for the charge pump current, the polarity of the VSYNC and the HSYNC, and the choice of the synchronization edge for the PLL), VCO (for the gain of the VCO, the resistance of the filter, and the MSB of the divider), DIVIDER (LSB of the divider), PHASEA and PHASEB (for the phase programming of clock signals). The choice of the different values for the registers will be developed in §3.2. The filter capacitances are fixed to $C_z = 40\text{nF}$ and $C_p = 150\text{pF}$. These two capacitances are valid for the working range of the PLL (from 12MHz to 80MHz).

A particular care should be taken for the clock outputs CKAOUT and CKBOUT. These two signals should not be loaded with more than 10pF, especially CKAOUT otherwise the sampling will be disturbed at high frequency. Then the CKAOUT signal is buffered with a 74ABT125 (IC13).

CKAOUT and CKBOUT are the output clocks of the PLL. These clocks are working at the same frequency. They can be shifted independantly by a phase shifter (either phase A or phase B). The phase shift is between 0° and 360° by steps of 11.25°. CKAOUT is the clock used for the ADC sampling.

2.2.3. Clamp pulse generation

To respect the functionality of the TDA8752, the clamp pulse can not happen at the same time as the HSYNC pulse (input of the PLL). Then, the clamp pulse is generated each line on the falling edge of the HSYNCl signal. HSYNCl signal is the equivalent of HSYNC signal but always with a positive polarity. The length of the pulse is fixed to n pixels, which is fixed to be < 48 by the LCD specification (see annex n°5).

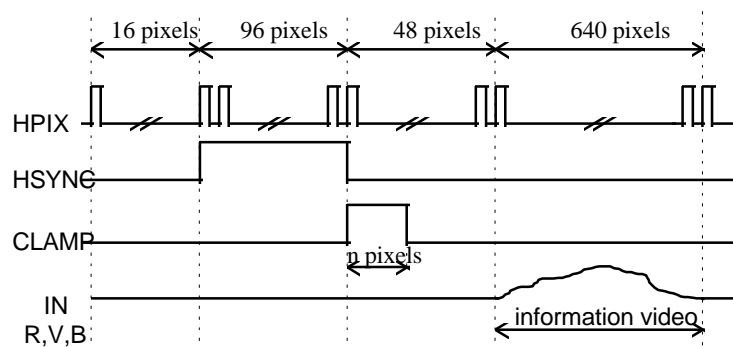


Fig.8 : Clamp timing diagram

The clamp pulse is generated by a multivibrator (74HCT221), which triggers the pulse on the falling edge of its input, which is the HSYNCl signal. The pulse length is defined by a RC network. A length of $1.2\mu\text{s}$ is chosen ($R = 2\text{k}\Omega$ and $C = 600\text{pF}$) which corresponds to 30 pixels when $T(\text{HPIX}) = 40\text{ns}$.

HSYNCl should have always a positive polarity, what ever is the input signal. It has been chosen to compare the signal to the average level of this signal (with the help of an exclusive OR, IC7). That means that if the polarity is positive, the pulse has a positive level 1 and the average level is 0. So it generates a signal with a positive polarity. And for a signal with a negative polarity, the pulse level is 0 whereas the average level is 1. It also generates a signal with a positive polarity.

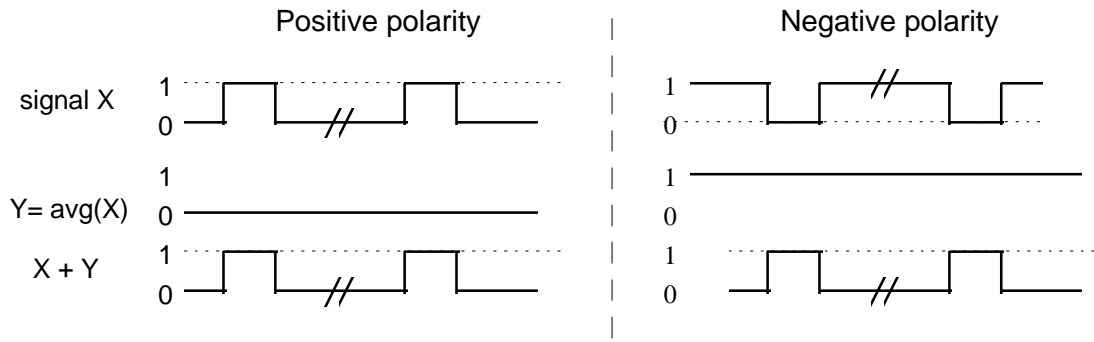


Fig.9 : polarity generation

To realize this function, a RC filter surrounded by two triggers (74HCT125D, IC6) will be implemented. And a 74F86 XOR gate will compare the two signals.

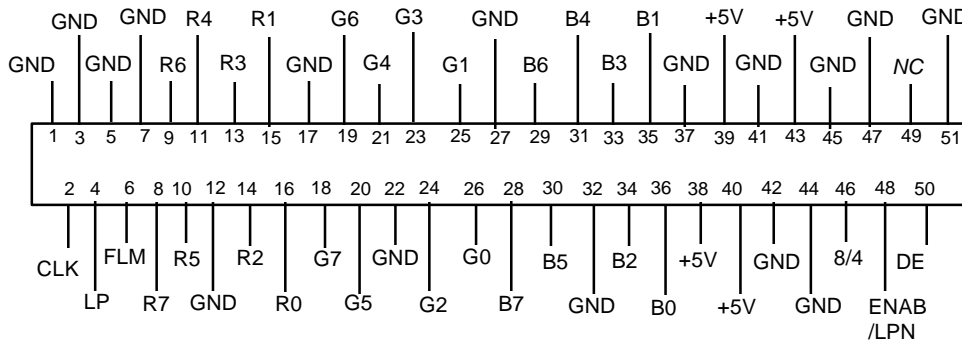
The time constant of the filters will be chosen in a such way, that the filters will cut 10 times below the input signal frequency. Consequently for a VGA configuration, the time constant is $\tau_h = 31.8 \mu s$ and $\tau_v = 16.7ms$.

The potentiometers P1 and P2 will allow flexibility on the resistor values.

2.2.4. External connections

The outputs of the converter have TTL level. To avoid timing problems for data acquisition and to buffer the signals, all the three times 8 outputs bits of the converter are connected to D Flip-flops (74ABT16283) with a resistance in serie to buffer the line, before going to the LCD connector. The converter outputs can be set in high state by switching K29 at 1 (the concerned pin is pin 87).

The connector (J5) is used for the connection between the outputs and the LCD. Its pinning is the following:



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In the following table will be explained the different signals, present on this connector (this is done in accordance with the LCD specification).

Pin	Name	Description	Pin	Name	Description
1	GND	ground	2	CLK	pixel clock
3	GND	ground	4	LP	Horizontal sync
5	GND	ground	6	FLM	Vertical sync
7	GND	ground	8	R7	red bit 7 (MSB)
9	R6	red bit 6	10	R5	red bit 5
11	R4	red bit 4	12	GND	ground
13	R3	red bit 3	14	R2	red bit 2
15	R1	red bit 1	16	R0	red bit 0 (LSB)
17	GND	ground	18	G7	green bit 7 (MSB)
19	G6	green bit 6	20	G6	green bit 6
21	G4	green bit 4	22	GND	ground
23	G3	green bit 3	24	G2	green bit 2
25	G1	green bit 1	26	G0	green bit 0 (LSB)
27	GND	ground	28	B7	blue bit 7 (MSB)
29	B6	blue bit 6	30	B6	blue bit 6
31	B4	blue bit 4	32	GND	ground
33	B3	blue bit 3	34	B2	blue bit 2
35	B1	blue bit 1	36	B0	blue bit 0 (LSB)
37	GND	ground	38	+5V	power supply
39	+5V	power supply	40	+5V	power supply
41	GND	ground	42	GND	ground
43	+5V	enable data mode non active	44	GND	ground
45	GND	ground	46	8/4	8 bit/color (HIGH) or 4 bit/color (LOW)
47	GND	ground	48	ENAB/ LPN	Line pulse interface
49	NC	not connected	50	DE	display enable
51	GND	ground			

The pin 48 is connected to the ground because the LCD is driven in LPN mode. A second connector (J8) is used to allow communication between the microcontroller and the TDA8752. Just some pins are connected on the demonstration board. The following table explains the different used pins:

Pin	Name	Description
7	P3.7	The P3.7 portout of the microcontroller is used to configure the communication type: 1 for I ² C and 0 for 3 wire communication.
9	P3.6	The P3.6 portout is directly connected to the SEN pin of the TDA8752. This pin is used as data validation pin for a 3 wire communication.
12	P3.1	The P3.1 pin (Txd pin for the microcontroller) is used as a clock wire for a 3 wire communication and so, is connected, via a multiplexer, to SCL pin of the TDA8752.
14	P3.0	The P3.0 pin (Rxd pin for the microcontroller) is used as a data wire for a 3 wire communication and so, is connected, via a multiplexer, to SDA pin of the TDA8752.
15	SDA	The SDA port of the microcontroller can be used directly for data transmission for I ² C communication. It is connected via a multiplexer to the SDA pin of the TDA8752.
17	SCL	The SCL port of the microcontroller can be used directly for a clock transmission for I ² C communication. It is connected via a multiplexer to the SCL pin of the TDA8752.
31	GND	Ground
32	GND	Ground
33	VCC	Power supply voltage (+5V)
34	VCC	Power supply voltage (+5V)

The used multiplexer is the 74HCT4053T. Just two of the three select inputs are used: S1 and S2. When S1 and S2 are at 0, the channels, which are switched on, are respectively 1Y0, 1Z and 2Y0, 2Z (communication 3W); when S1 and S2 are at 1, the channels which are switched on, are respectively 1Y1, 1Z and 2Y1 and 2Z (communication I²C).

On the board, an external clock can be used, instead of the internal clock generated by the PLL. This clock is connected on the connector J4 (CEXT). To use an external clock, the register PHASEA must be configured as indicated in the TDA8752 specification (that is to say: the bit Cka at 1). More explanations on the registers will be given in the chapter 3.

2.2.5. External components

Some external components are very important and some attention needs to be taken. The decoupling of the pins xBOT, xGAINC, xCLP, xDEC, xIN, and the decoupling pins for the power supply voltages should be as near as possible to the chip. This recommendation is very important for the pin xBOT. If there is a too big self between the output and the decoupling capacitor, this causes oscillation.

The VREF pin should be at a very stable voltage of 2.5V with a maximum variation of 100ppm/°C in order to ensure the amplification precision over the temperature range. In the application a TL431C is employed; this component has a variation of 17mV maximum over the temperature range of 70°C.

On the pins xAGC nothing should be connected. The pins TCK and TCO should be connected to the ground. These two pins are used for the test only.

2.3. SUPPLY VOLTAGES

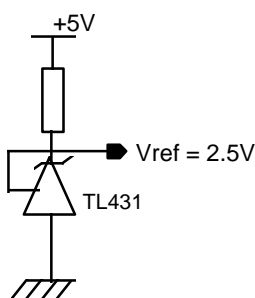
All the ADC supply voltages are derived either from the on board 7805 regulator (IC5), or from any +5V supply voltages, and are well decoupled from each other by the means of LC filters.

There are 7 supply voltages, which are :

- +5VAN_1: analog supply voltage of +5V for the analog part of the R, G, and B channels (pins 11, 19, 27).
- +5VAN_2: analog supply voltage of +5V for the PLL part (pin 99).
- +5VA: output buffer supply voltage for the PLL. It is a +5V supply voltage (pin 85).
- VDDO: output buffers supply voltage of +5V for the R, G, and B channels (pins 59, 69, 79).
- VDD: supply voltage for the LCD screen: +5V.
- VCC1: digital supply voltage for the digital part of the TDA8752 (pin 95).
- VCC: digital supply voltage of +5V for all the other logic components and for the bus (pin 40).

The input of the regulator is a +8V supply voltage.

All the reference voltages for the ADC part of the TDA8752 are internal. But for the amplifier and the clamp part, a VREF voltage must be provided. It has to be a very stable 2.5V supply voltage, which is supplied by a TL431C connected as a diode as follow:



2.4. SWITCHES AND CONNECTORS USES

2.4.1. Description

The following table resumes firstly all the switches and secondly the connectors present on the board. It will explain also their uses.

Name	Description
K1 to K8	These switches allow the programming of the counter IC8 for the LCD vertical synchronization. The LSB bit is driven by K8 and the MSB by K1. For example to count up to 11, the switches K8, K7, K5 are connected to +5V.
K9 to K16	These switches allow the programming of the counter IC7 for the LCD horizontal synchronization. The LSB bit is driven by K16 and the MSB by K9.
K17 to K24	These switches allow the programming of the counter IC9 for the LCD horizontal synchronization. The LSB bit is driven by K24 and the MSB by K17.
K25	The chosen supply voltage is delivered either by the regulator 7805 or by an external supply voltage (VEXT).
K26	This strap allows the use of the INV pin at a frequency of $\frac{1}{2}$ of the vertical synchronization frequency. This allows to read once the even pixels and after the odd pixels at a sampling frequency of 80MHz. The effect will be nearly the same as an image sampled at 160MHz (with half frame rate).
K27	HSYNC is synchronized by CKBOUT clock to generate HSYNCI to drive the TDA8752 and to create the LP pulse.

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K28	This switch controls the power off of the TDA8752. At low level (ground), the circuit is active. At high level (+5V), the power is cut off. The power consumption is then 87 mW.
K29	The outputs of the TDA8752 are in high impedance or not: at high level, they are in high impedance.
K30	Connect the second flip-flop to get rid of setup and hold timing problem.
K31 to K32	Theses two switches are used for the TDA8752 I ² C address programming on the pins ADD1 and ADD2.
K33	To allow a bus communication (I ² C or 3 wire), the switch must be at low level, otherwise no communication is possible.
K34	To select SDA coming either from the multiplexer output or directly from the I ² C board communication.
K35	To select SCL coming either from the multiplexer output or directly from the I ² C board communication.
K36	Allow the choice of the mode of the LCD screen: either, it is at high level, and the LCD screen is defined with 8 bits/color or it is in low state and the definition is of 4 bits/color.
K37	This switch is used to switch off the LCD screen independently of the board.
J1	This connector is the supply voltage: either +8V or +5V.
J2	VGA connector to drive the data from the PC to a monitor to have the possibility to compare the two images, one from the LCD and the other from the monitor.
J3	VGA connector to drive the data from the PC to the chip TDA8752.
J4	Connector for an external clock (CKEXT).
J5	51 pins connector to the LCD screen.
J6 and J7	Connectors used for the I ² C bus board connection (with SDA, SCL, VDD, GND).
J8	34 pins connector to the microcontroller.
TP13 and TP14	A strap between these two points allows the connection of the I2C3W pin at high level (I ² C communication).
TP13 and TP12	A strap between these two points allows the connection of the I2C3W pin at the microcontroller pin to allow a communication by using the microcontroller board.

2.4.2. Initial settings

On figures 10 and 11; the initial settings of the switches are represented in configuration with microcontroller board and in configuration with I²C board.

All the switches for the vertical and horizontal synchronization of the LCD screen are configured in accordance with the specification of the LCD screen LDH102T-20 from FPD.

For the vertical synchronization, the counter IC8 has to count down from $m=34$. Consequently the switches K3, K7 and K8 must be at +5V and the others at 0V. For the horizontal synchronization, the relation $n1+n2=128$ must be followed, and consequently, $n1=n2=64$. Then the switches K10 and K18 are switched on.

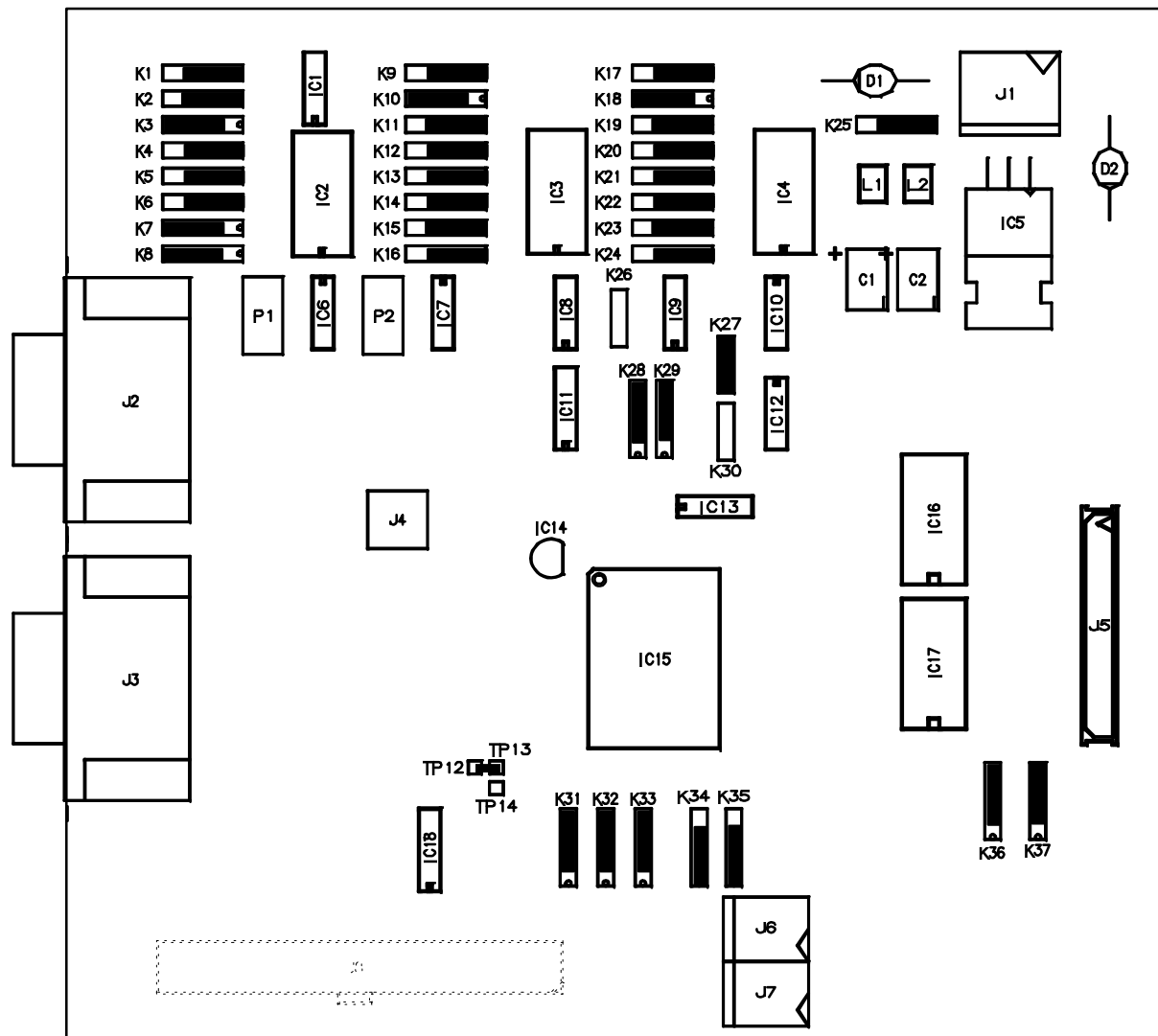
Firstly, the strap K26 is not used, the switches K28, K29, K33 and K37 are at 0V. The chosen supply voltage is coming from the voltage regulator, then the switch K25 is on the "REG" position.

For the I²C communication, the address of the component must be fixed. For a communication with just 1 chip, the bits ADD1 and ADD2 are connected to the ground. Then the switches K31 and K32 are at 0V.

The switch K36 for the LCD definition is connected at +5V to have an 8 bits/color definition. The strap on K27 is on to generate HSYNCI.

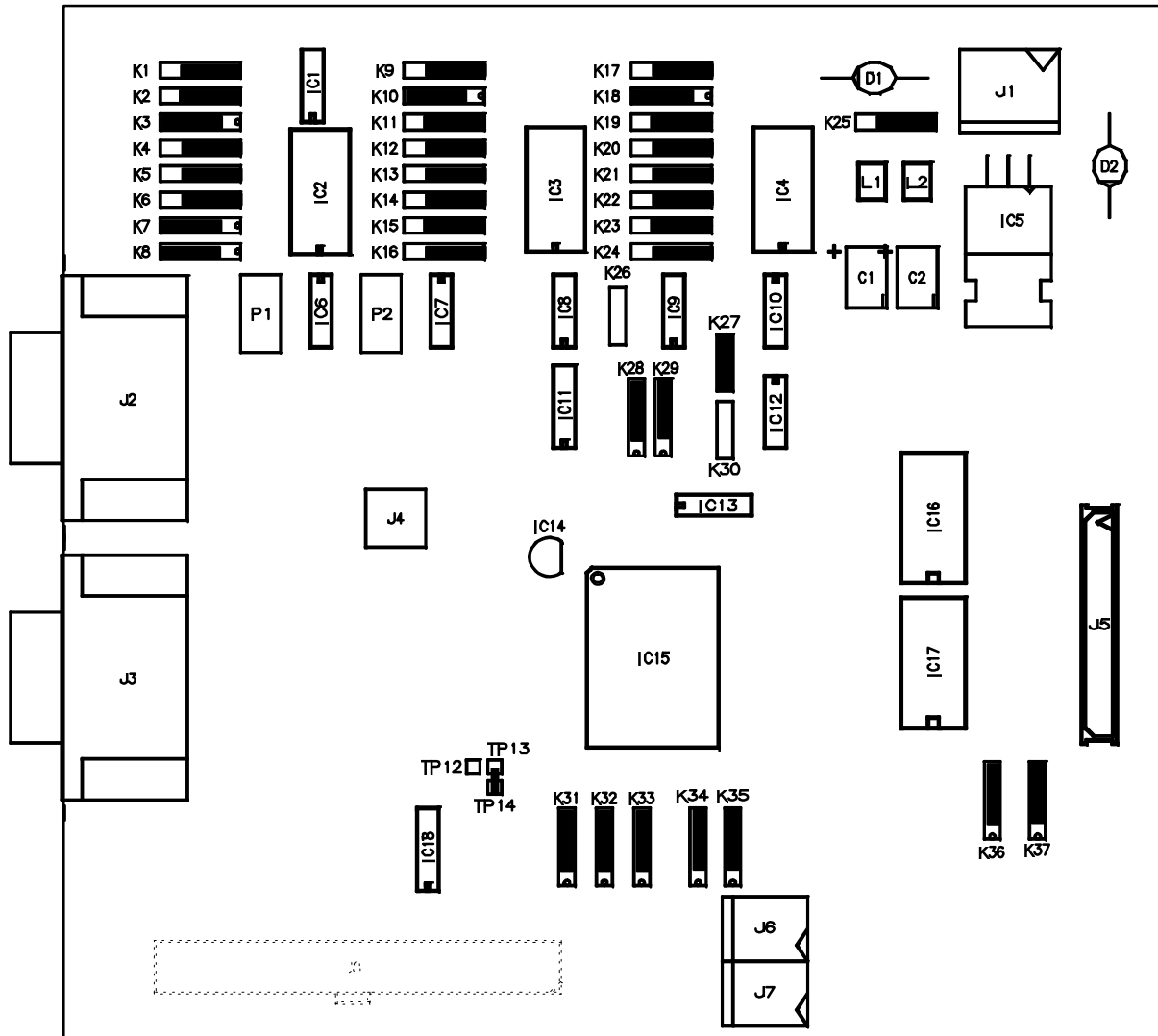
When the microcontroller board is connected, the switches K34 and K35 are configured to have SDA and SCL coming from the multiplexer. A strap should be put between TP13 and TP12 (see Fig.10).

When the programming of the registers is done via the I²C board, the switches K34 and K35 should be positioned to have a connection between the TDA8752 and the connectors J7 and J8. A strap links TP13 and TP14 to force the pin I2C3W to 1 (see Fig.11).



DEM08752-3 PCB-No: 514

Fig.10 : Switches position for initial settings with microcontroller board.



DEM08752-3 PCB-No: 514

Fig.11 : Switches position for initial settings with the I²C board.

3. TDA8752 SETTINGS

In the first section will take place a short description of how works the TDA8752 for the different controls. The settings of the registers are described in the second section.

3.1. HOW WORK

3.1.1. Clamp and gain

There are in the chip 3 equivalent channels, which are R, G, and B. Three independent clamp circuits and three independent variable gain amplifiers are used respectively to clamp the video input and to provide, for each channel, a full-scale input range signal to the 8 bit ADC. One channel is represented in figure 12.

The clamp is adjusted during the clamp pulse. This pulse is provided externally and it has to be after the horizontal synchronization pulse (for example HSYNC). The clamp pulse could be shorter than it is in the demonstration board: around 400nS can be OK.

This clamp is a parallel clamp with a high precision because the clamp control is done at the output of the AGC (then it always takes care of the gain), and with a quick reaction (because the clamp level is fixed at the input of the ADC).

The gain is adjusted during the video synchronization pulse (HSYNC). During this time, the output of the input multiplexer, which is 1/16 VREF, is digitized by the ADC and then compared to the programmed code in the coarse register. No relation exists between the input and the ADC outputs during this pulse. The stability (at $\pm 0.1\text{LSB}$) is achieved when :

$$\text{The output code of the channel} = \text{coarse code} + 128 \pm 1.$$

The FINE gain correction is done by an adjustment of VREF.

To have a good stability of the gain versus the temperature, it is useful to have a VREF stable in temperature.

3.1.2. PLL

All the PLL parameters can be programmed like: the divider ratio (to have the correct pixels number), the gain of the VCO, the current of the charge pump current, the resistance of the loop filter.

Some extra bits can be controlled too :

- * the VLEVEL and HLEVEL bits used to define if the signals VSYNC and HSYNC have a negative or positive polarity (if the bit is at 0, the polarity of the signal is positive).
- * the edge bit which allows to synchronize the PLL on a rising edge of CKREF (if bit = 0) or on the falling edge of CKREF (if bit = 1).
- * the UP and DO bits do not have to be used in the normal use of the chip. They have to stay at 0, which is the default value.

To reduce the jitter of the PLL, a good compromise should be found between the VCO gain (bits Vco1 and Vco2), the charge pump current (bits Ip0, Ip1, and Ip2), and the resistance of the filter (bits Z0, Z1, and Z2).

To have control on the sampling moment of the data, and to have the possibility to control external clock, two phase shifters are implemented in the PLL block and controlled by the registers PHASEA and PHASEB. These phase shifters are working from 0° to 348.75° by steps of 11.25° (programming of the bits PAi and PBi). In the demoboard, the phase shifter B allows the control of the horizontal synchronization of the LCD screen. In fact, it controls the LP signal.

In these registers exist two bits Cka and Ckb: the first one is programmed at 1 to use an external clock and not the PLL, the second one is used to switch on or off the CKBOUT clock (when the bit Ckb is at one, the CKBOUT clock is available on the pin CKBOUT).

3.2. REGISTER SETTINGS

3.2.1. Clamp and gain

For the clamp, the registers OFFSETR, OFFSETG, OFFSETB must be programmed. These registers are programmable on 8 bits from the ADC code -63.5 to the code 64 by steps of $\frac{1}{2}$ LSB. A way to control the contrast is to change the clamp level: for a code below 0, the picture will be darker than for a clamp level above 0. The default value of these clamp registers is 127 (for a clamp code at 0).

For the gain, two registers per channel (RED, GREEN, BLUE) exist to control the gain. The COARSE register allows to control the gain within 4 LSB and the FINE register with a precision of $\frac{1}{2}$ LSB.

The coarse gain is controllable in order to have the possibility to be full scale at the input of the ADC with a signal of 1V peak to peak. The coarse gain is in a range of 0.825 to 2.5, which allows to have a signal at the input of the chip from 0.4V peak to peak to 1.2V peak to peak. If the input signal has an amplitude bigger than 1.2Vp.p or if the used gain gives an input of the ADC bigger than 1V p.p, the output stages of the voltage gain amplifier will be saturated, and the output data of the chip will not be correct. The range in which the coarse gain can be programmed is between 32 (20 in hexadecimal) and 99 (63 in hexadecimal).

The default value for the coarse gain is 32, equivalent to a gain of 0.825. The control of the gain will allow a control of the brightness of the screen.

3.2.2. PLL

The default programming of these registers is: 4 (04 in hexadecimal) for the CONTROL register, 97 (61 in hexadecimal) for the VCO register, 144 (90 in hexadecimal) for the DIVIDER register. These values correspond to a charge pump current of 100 μ A, to a VCO gain of 15MHz/V, to a resistance of 16k Ω , to a total divider ratio of 800. These parameters are the "normal" parameters for a VGA signal. For a jitter optimization, it will be better to program a higher charge pump current and to reduce the resistance of the loop filter: VCO gain of 15MHz/V, charge pump of 200 μ A and resistance of 2k Ω .

In the case of a SVGA signal (50MHz clock), the programming would be a VCO gain of 30MHz/V, a charge pump current of 700 μ A and an impedance of 2k Ω . For a signal around 80MHz, the VCO gain will be 60MHz/V, the charge pump current 700 μ A, and the resistance 4k Ω . Do not forget to adapt the divider ratio to the number of pixels you want. The stability of a picture depends of this parameter too.

To fix correctly the PLL parameters, the first to choose is the divider ratio. Then, the VCO gain (Ko) has to be chosen as following: generally, the smallest Ko in the frequency range of the application is chosen (see the following table).

Bit Vco1	Bit Vco0	VCO gain (Ko) (MHz/V)	Frequency Range (MHz)
0	0	15	2.5 to 25
0	1	30	5 to 50
1	0	60	8 to 80
1	1	100	15 to 150

After with a damping factor (ξ) of 1.5, and a natural PLL bandwidth = $W_n = F_{ref}/10$, the following equation can be solved and Ip and R can be calculated.

$$W_n = \sqrt{\frac{K_{olp}}{(C_z + C_p) N}}$$

and

$$W_z = \frac{1}{R \times C_z} \text{ and } x = \frac{1}{2} \times \frac{W_n}{W_z}$$

To use the demonstration board, it is important to set at 1 the CKB bit in order to produce the LP signal. The programmed default value is 0 for the PHASEA and for the PHASEB registers.

When the phase is not correctly adapted, an aliasing effect or watering effect appears on the picture. The phase shift has then to be changed and adapted. When it is adapted for a "hard picture" (like a pixel on pixel off picture), it should not be changed at any time.

4. INTERFACE BOARDS TO DRIVE THE TDA8752

As explained in the pages before, it is possible to drive the TDA8752 in two different ways: either by using the I²C interface board (which is the simplest way to program the registers), or with the help of the microcontroller board, which allows two types of communication (I²C or 3 wires data transmission).

4.1. USE OF THE I²C BOARD

To use the I²C single master interface board (see annex 4) is an easy way to change the registers values of the TDA8752. This will be done only by I²C communication with the help of a single master interface, a PC, and the software for PHILIPS I²C bus.

4.1.1. The interface board

This board has just some 10K resistors, some capacitors for the supply decoupling, a 74LS05, and two connectors: one to connect the interface board to the parallel output port of the PC and the second one to connect the interface board to the demonstration board (SDA, SCL, VDD, GND). The schematic of the interface board is available in the annex 4.

4.1.2. The I²C software

It is possible to program the different registers of the TDA8752 using the associated I²C software. To run the program, follow the instructions given in annex 4. After giving the instruction "go", choose in the menu the choice named "universal transmitter/receiver" (more explanations on page 7 of the annex 4). To modify the registers, follow the I²C protocol:

SEQUENCE								
S ⁽¹⁾	IC ADDRESS	W	A ⁽²⁾	SUB ADDRESS REGISTER 1	A	DATA REGISTER 1	A	P ⁽³⁾

S⁽¹⁾: Start condition.

A⁽²⁾: Acknowledge bit, generated by the TDA8752.

P⁽³⁾: Stop condition.

With the bits ADD1 and ADD2 connected to the ground, and considering that the data are only written (W) in the TDA8752 registers, the IC address is 98H. The following table resumes the IC ADDRESS function of ADD1 and ADD2.

ADD2	ADD1	IC ADDRESS
0	0	98 H
0	1	9A H
1	0	9C H
1	1	9E H

The sub address is indicated in the TDA8752 specification. It is also programmed in hexadecimal.

REGISTER NAME	SUBADDRESS
OFFSETR	00 H
COARSER	01 H
FINER	02 H
OFFSETG	03 H
COARSEG	04 H
FINEG	05 H
OFFSETB	06 H
COARSEB	07 H
FINEB	08 H
CONTROL	09 H
VCO	0A H
DIVIDER (LSB)	0B H
PHASEA	0C H
PHASEB	0D H

The register data values are also programmed in hexadecimal and sent to the TDA8752 by using F3. Then just one setting will be sent to the chip. Consequently, it is equivalent to work in mode 0 for the TDA8752 (see the specification): the bit A4 of the subaddress is then at 0, which is in accordance to the table above.

A list of errors is in the annex 4. The most common errors are: no connection between the PC and the I²C interface board, no supply voltage for the I²C bus, or a wrong IC address programming (no acknowledge will be received).

This will allow a very easy programming of the registers, just by using the I²C communication.

Do not forget to program at 1 the bit Ckb (in the PHASE B register) in order to have the possibility to generate the signal LP and FLM.

4.2. USE OF THE BOARD WITH THE MICROCONTROLLER

A short description of the board (n°453) named microcontroller board will illustrate the schematic in annex 2. This board will allow to use either the I²C or 3 wires communication to program the 14 existing registers. How to use this board will be described subsequently.

4.2.1. Description

This board is constituted of four main components.

An LCD module gives the possibility to display which register will be programmed, with which values. It will give a visible control for the chip programming. This LCD module is a VIM-878-DP, with 8 digits of 16 segments. The scheme drive of this display is a multiplex scheme. Consequently the LCD driver must be compatible: a PCF8576 is chosen. The option for driving this LCD is a multiplex mode 1:4 in the PCF8576 use.

The chosen microcontroller is an 8 bits microcontroller, 80C51, which has enough capacity to control just 14 registers. The port P2 is connected to the keyboard. The keyboard is managed by the 80C51 by a pulling method. All the other ports are connected to the connector 34 points. In this application just the SDA and SCL ports are used for the I²C communication, the P3.0 (Rxd) and P3.1 (Txd) transmit respectively the data and the clock for a 3 wires communication. The bit P3.7 will be forced automatically by the microcontroller to 1 for a I²C communication and 0 for a three wire communication. This bit is directly connected to the pin I2C/3W. When the 3 wire communication mode is chosen, the data validation is done by a pulse automatically generated on SEN pin.

An EEPROM (PCD8598) is installed on the board to give the possibility to store a certain configuration of the register. To find again the configuration, the EEPROM content should be read by the TDA8752.

The program is explained and described in annex 3.

4.2.2. Instructions for use

The way to make modifications in registers, is described in the following figures. The registers are classified in different sections as follow:

- "RED" section: OFFSETR, COARSER, FINER.
- "GREEN" section: OFFSETG, COARSEG, FINEG.
- "BLUE" section: OFFSETB, COARSEB, FINEB.
- "CLOCK" section: CONTROL, VCO, DIVIDER, PHASEA, PHASEB.
- "EEPROM" section which has subsections: PAGE1, PAGE2, PAGE3, PAGE4.

Each of these subsections has two registers: READ, WRITE.

This last section is not related to the TDA8752. On the microcontroller board an EEPROM is used to give the possibility to memorize some configurations.

The representation of the keyboard is shown in the following Fig.13 :

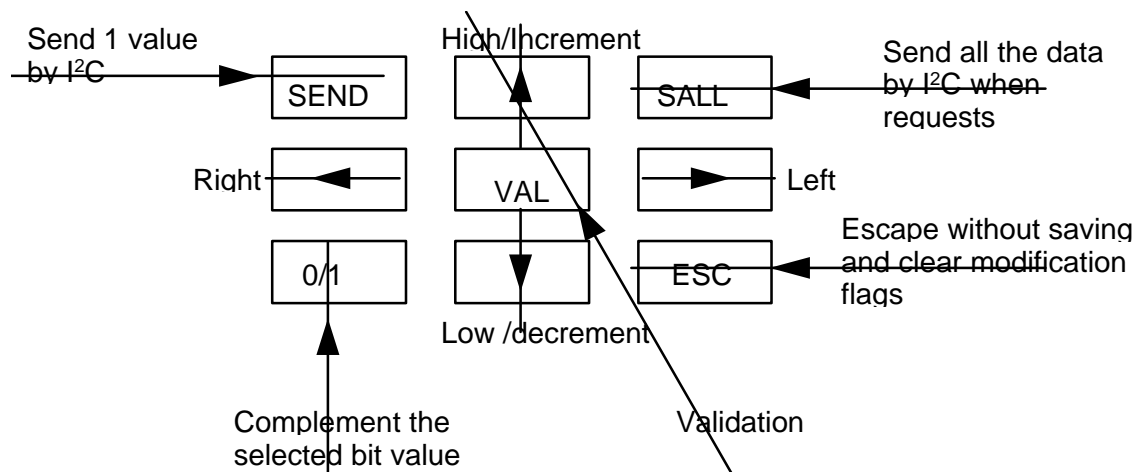
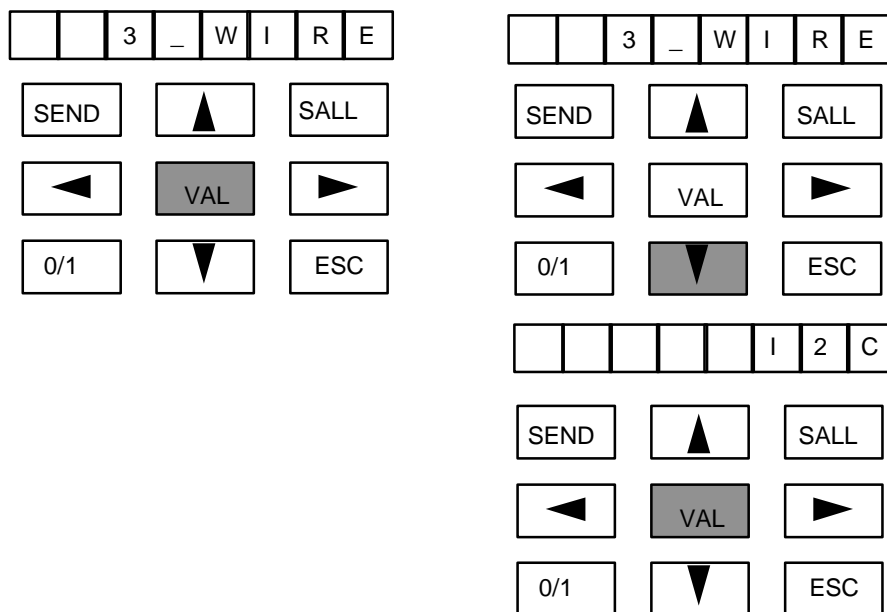


Fig.13 : Definition of the microcontroller keyboard

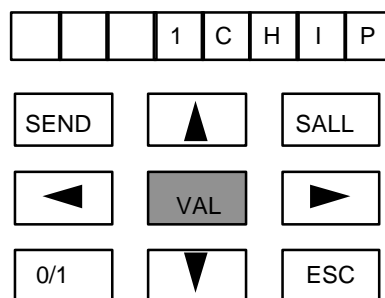
In the following figures, the grey box corresponds to the key to press to realize the described action, and the text, at the top of the figures, is the one which is readable on the 8 digits LCD display.

To allow the generation of the LP and FLM signals, the clock CKBOUT should be active. Then, the first thing is to modify the Ckb bit of the PHASE B register. The explanation will be given on this example.

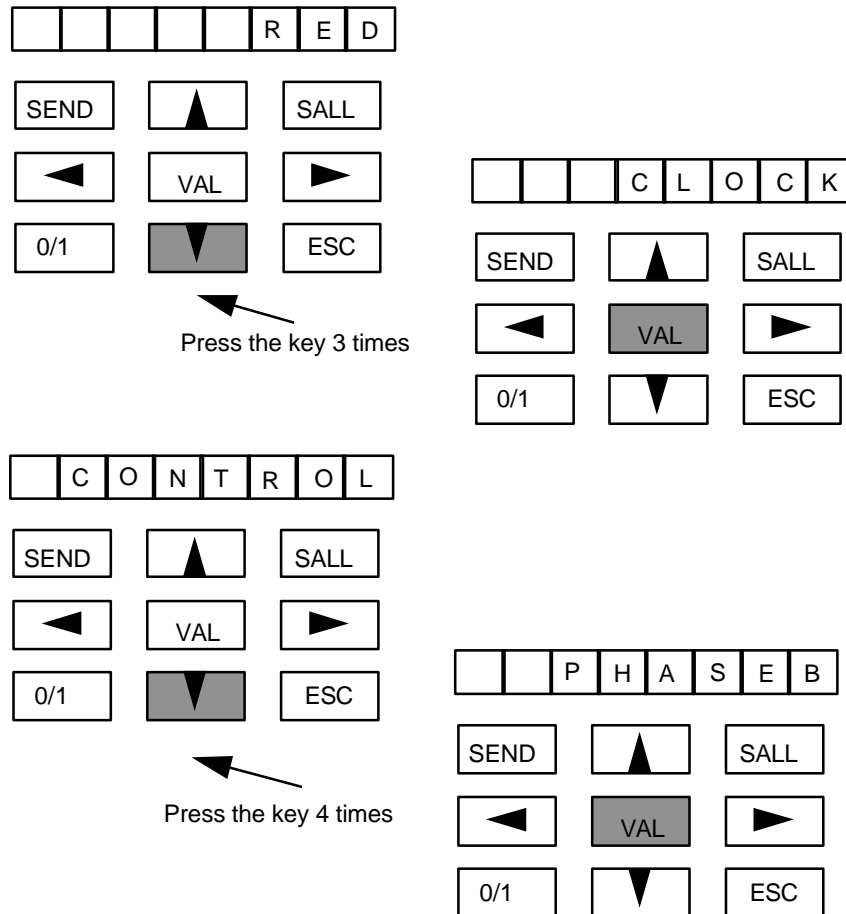
1- Switch on the microcontroller board: the 5V is directly connected to the VCC of the main board. Then choose the communication mode to use (either 3 wire or I²C).



2- Choose to work with one chip or two chips. With this board , it is just possible to use one chip.

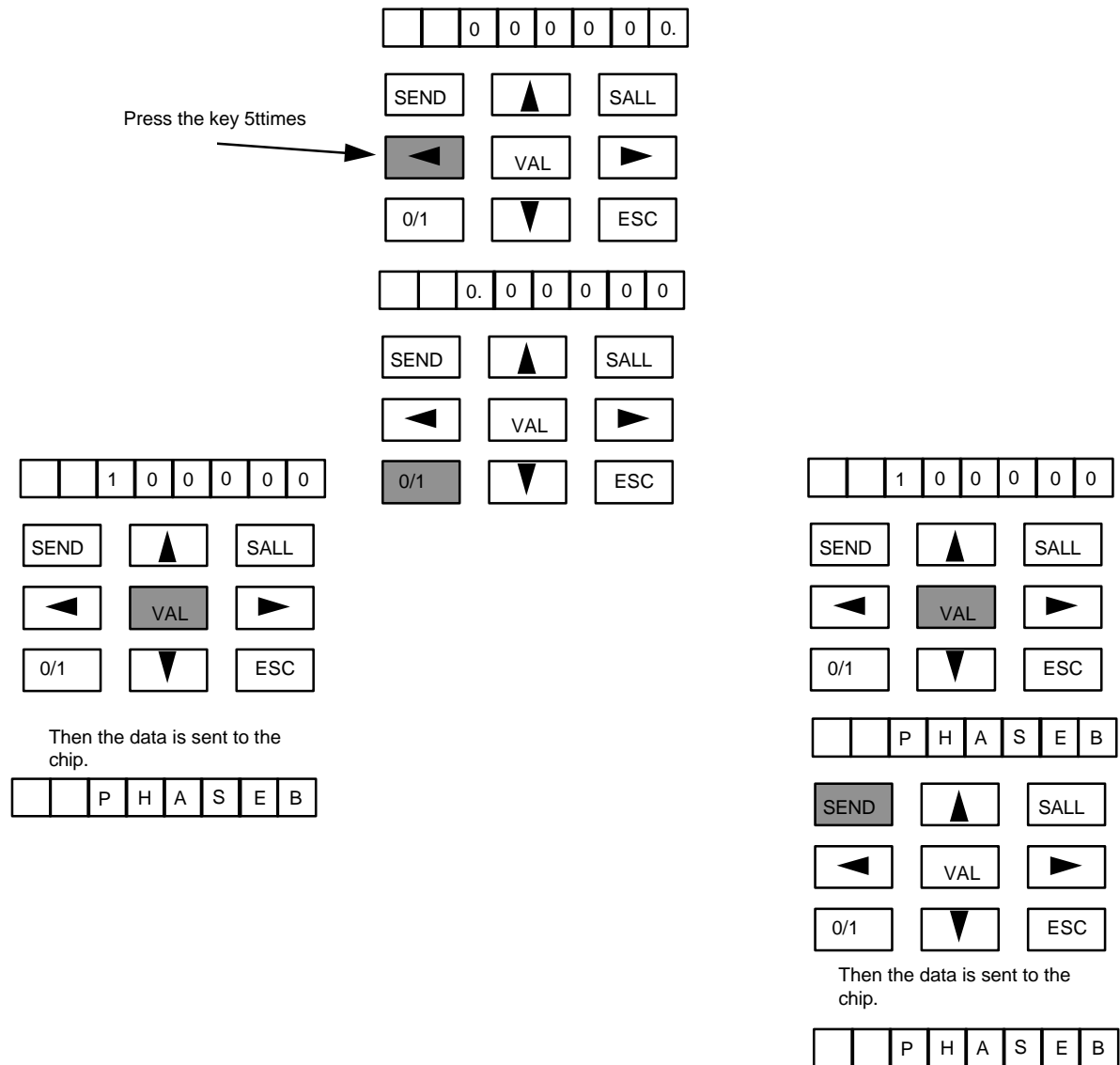


3- Select the section in which the register you want to modify is. In this example, the register PHASE B is in the CLOCK section.



4- Program the bit Ckb to 1 and send the data to the chip (right: it is with a 3 wire communication, and on the left: with a I²C communication).

**Triple high speed analog to digital converter
for LCD drive. TDA8752**



Remarks :

- Before validating the value of the register you want to modify, if finally you do not want to make changes, just press the key ESC.

- If you are using an I²C communication and you change all registers, do not use the key SEND for each register. You just have to validate (VAL) and when the 14 registers are programmed you will have to answer to the question: SEND ALL? If yes, just press the key SALL and all the registers will be programmed at the same time.

- If you want to memorize or read data in the EEPROM, go in EEPROM menu, choose the page, and what you want to do: read or write.

5. CONCLUSION

All the documentation used for the realization of the board are given in the annex :

- The electrical schematics of the demonstration board in annex 1.1
- The layout schematics in the annex 1.2.
- The nomenclature in the annex 1.3.

The specification of the TDA8752 , of the LCD screen (see annex 5) and of the I2C interface board and software (see annex 4) are useful to drive this demoboard.

An other demonstration board is under preparation ; it will give the possibility to drive several kinds of LCD, and also the possibility to work with two TDA8752 at higher frequency like 160 MHz.

6. ANNEXES

ANNEX 1 : BOARD REALISATION

- 1.1 : ELECTRICAL SCHEMATICS
- 1.2 : LAYOUT
- 1.3 : PART LIST

ANNEX 2 : MICROCONTROLLER BOARD SCHEMATIC

ANNEX 3 : MICROCONTROLLER SOFTWARE

ANNEX 4 : I²C USER SOFTWARE

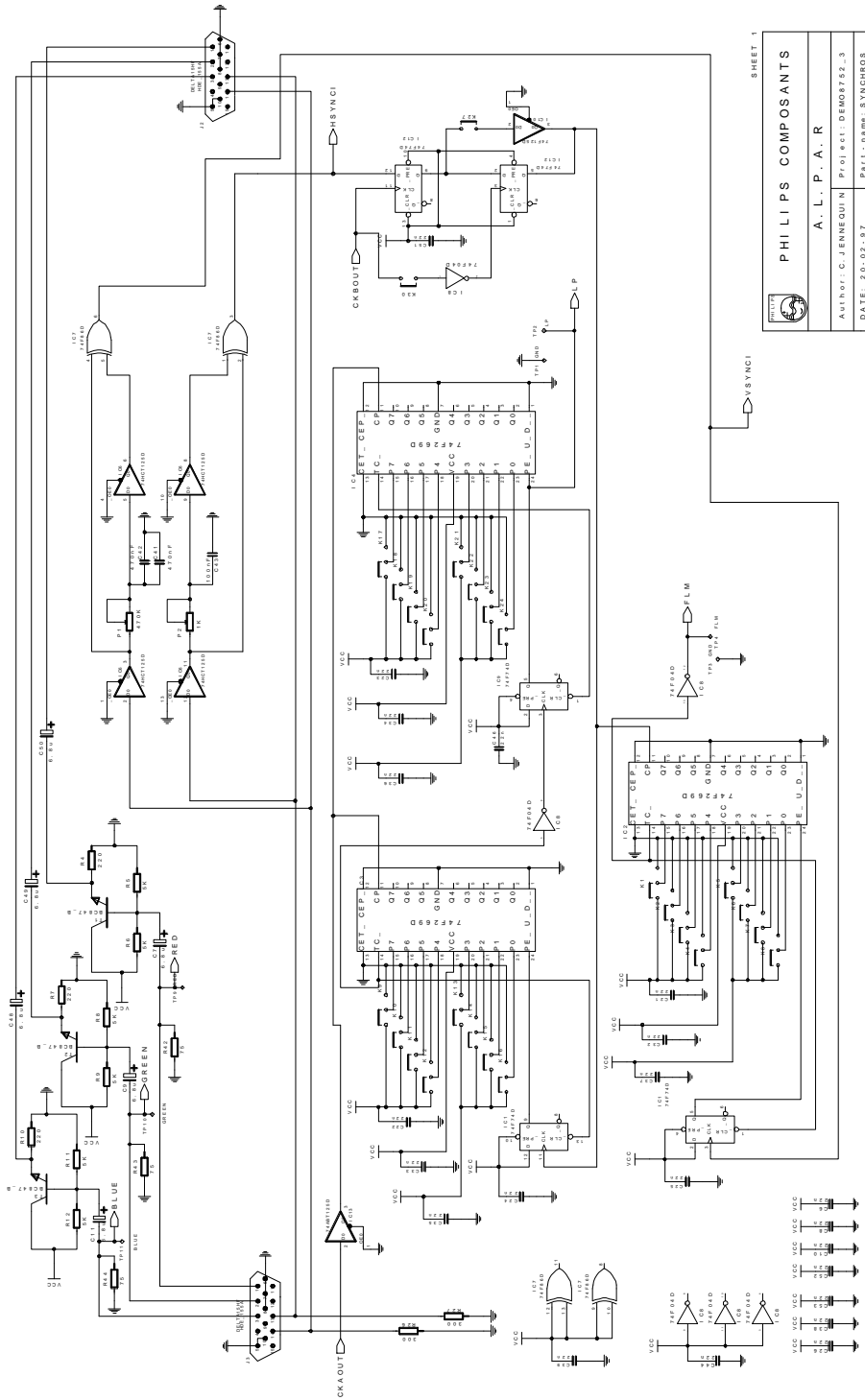
ANNEX 5 : LCD SPECIFICATION

ANNEX 1

BOARD REALISATION

1.1 ELECTRICAL SCHEMATICS

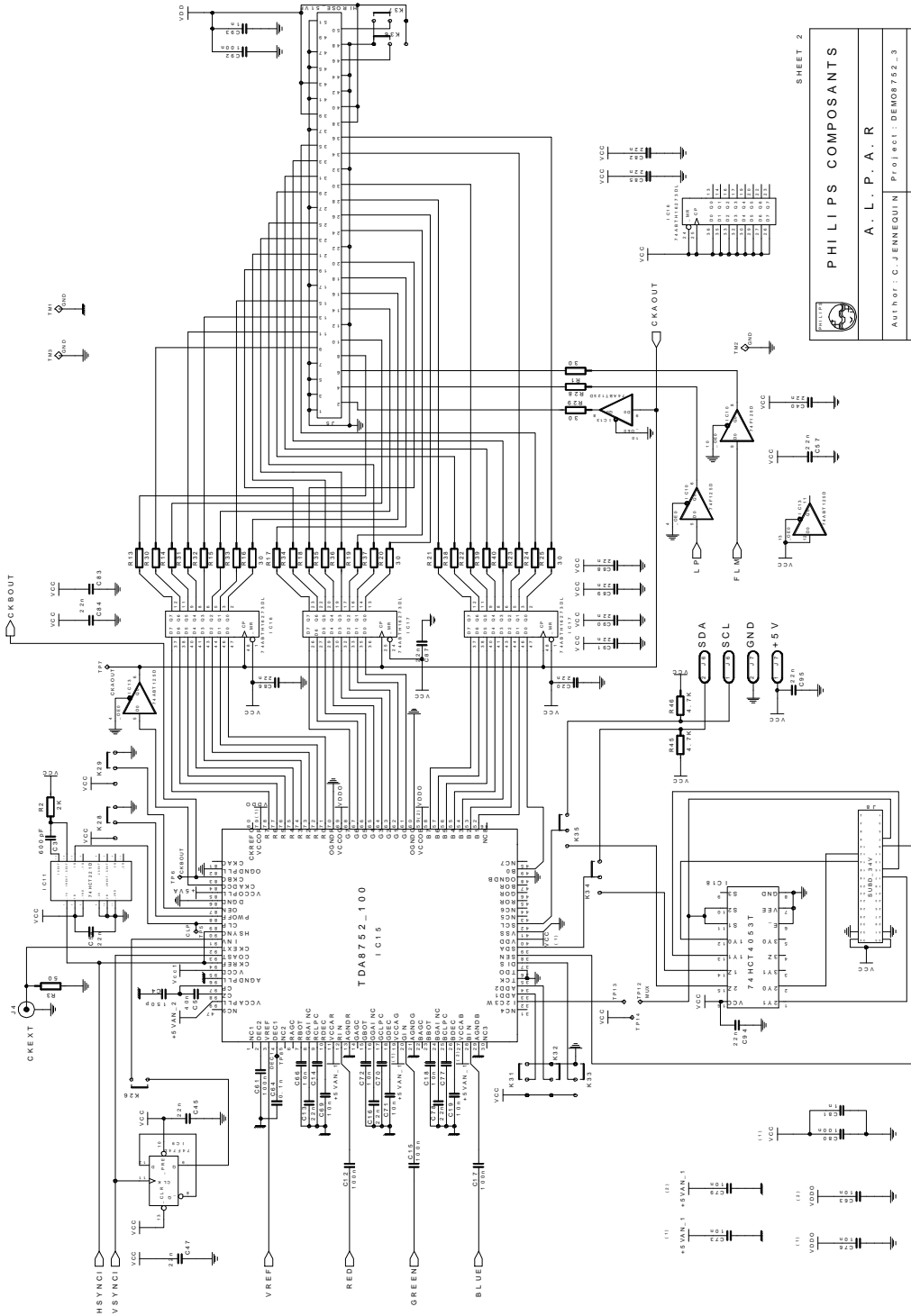
**Triple high speed analog to digital converter
for LCD drive. TDA8752**



SHEET 1

PHILIPS COMPOSANTS
A. L. P. A. R
Auteur: C. JENNEQUIN Projet: DEMO8752_3
DATE: 20-02-97 Part: name: SYNCHROS

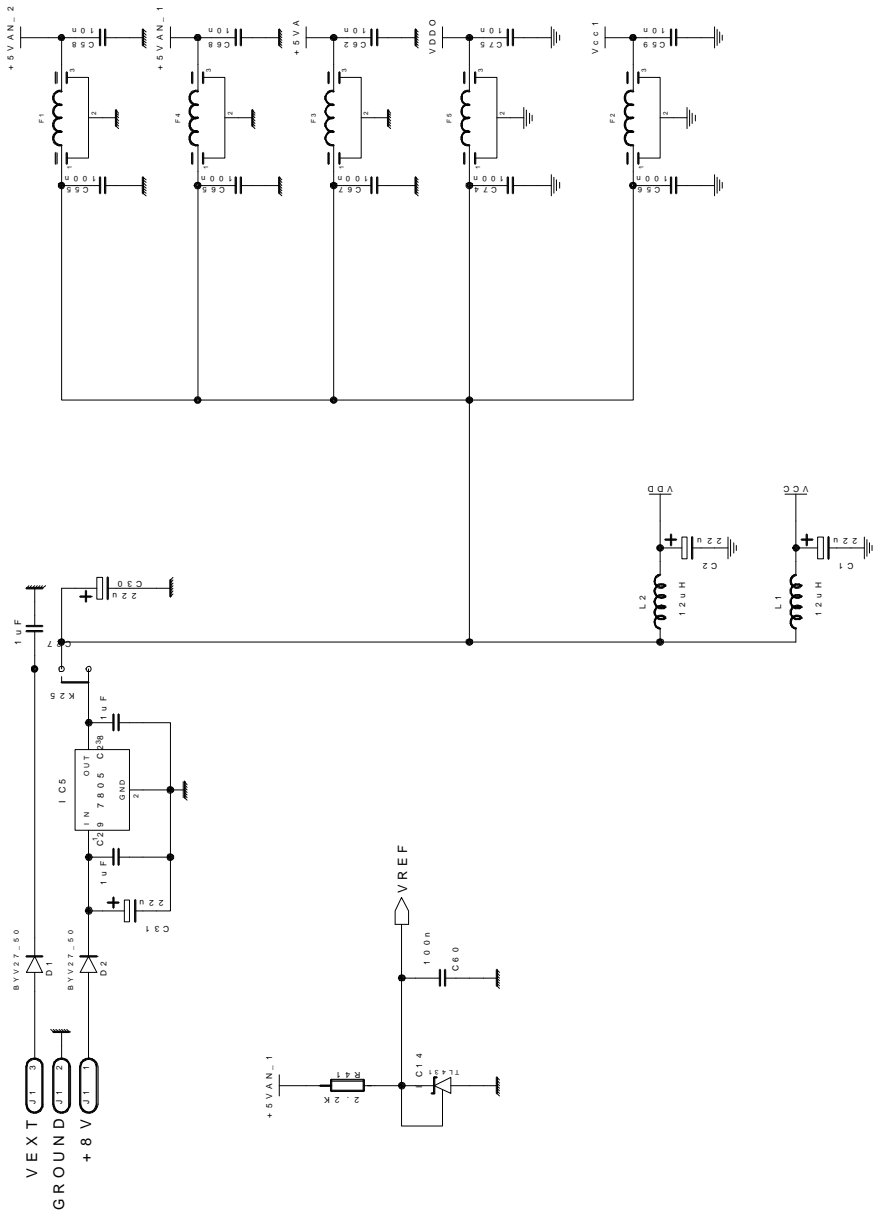
**Triple high speed analog to digital converter
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
SHEET 2

PHILIPS COMPONENTS
A. L. P. A. R.
Author: C. JENNEDIN Project: DEMO8752_3
DATE: 10-02-97 Part-name: CONVERSION

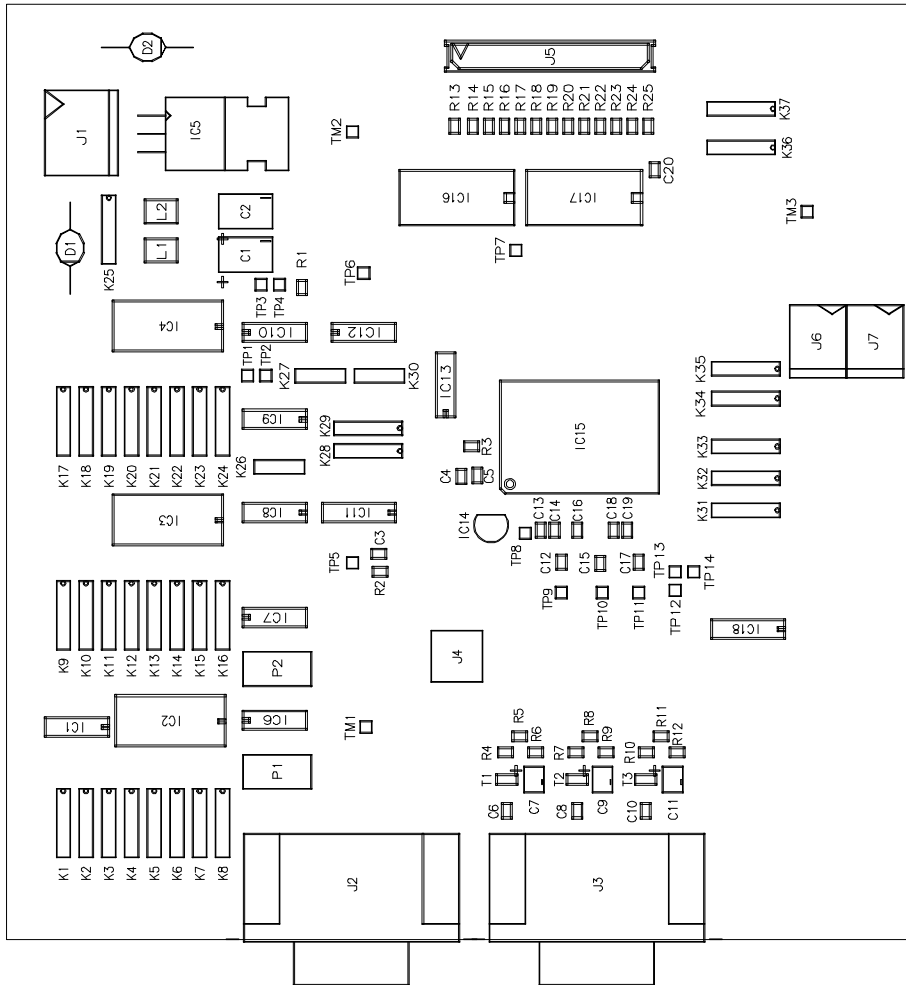
**Triple high speed analog to digital converter
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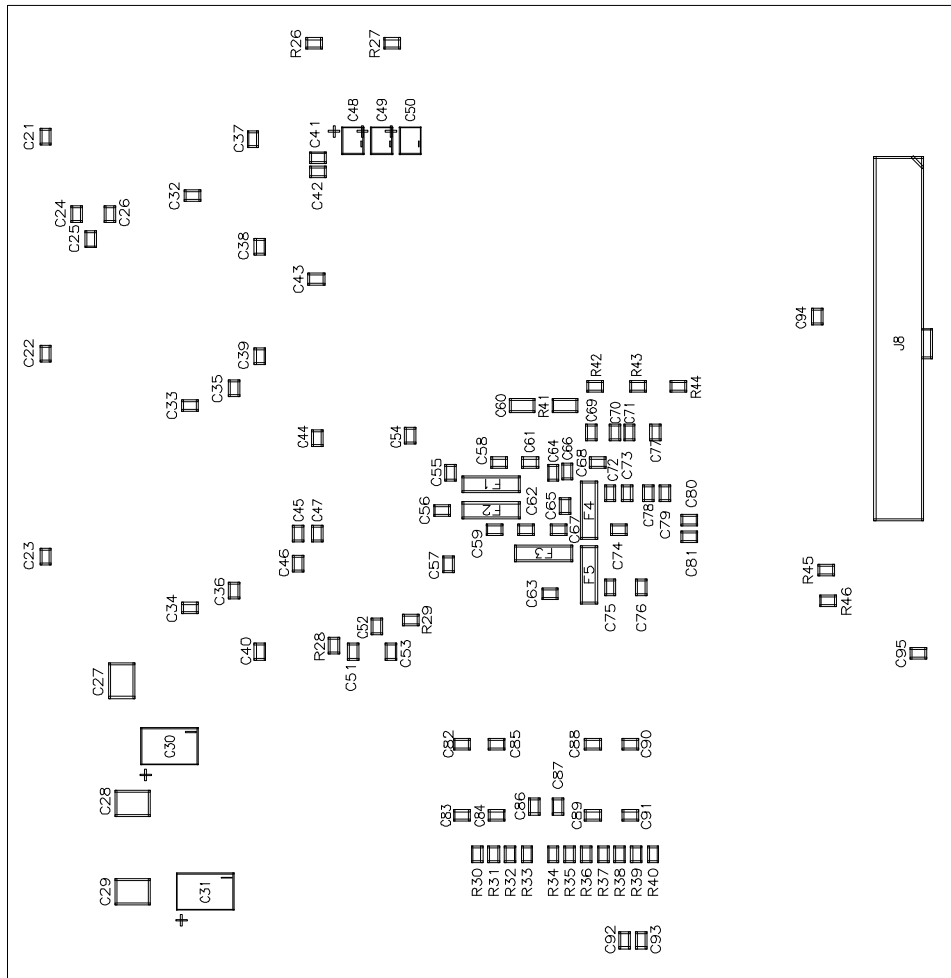
SHEET 3

 PHILIPS COMPOSANTS	
A. L. P. A. R	
Author : C. JENNEQUIN	Project : DEMO8752_3
DATE : 20-02-97	Part-name : SUPPLIES

1.2 LAYOUT



DEM08752-3 PCB-No: 514
EQUIPMENT FACE ELEMENTS



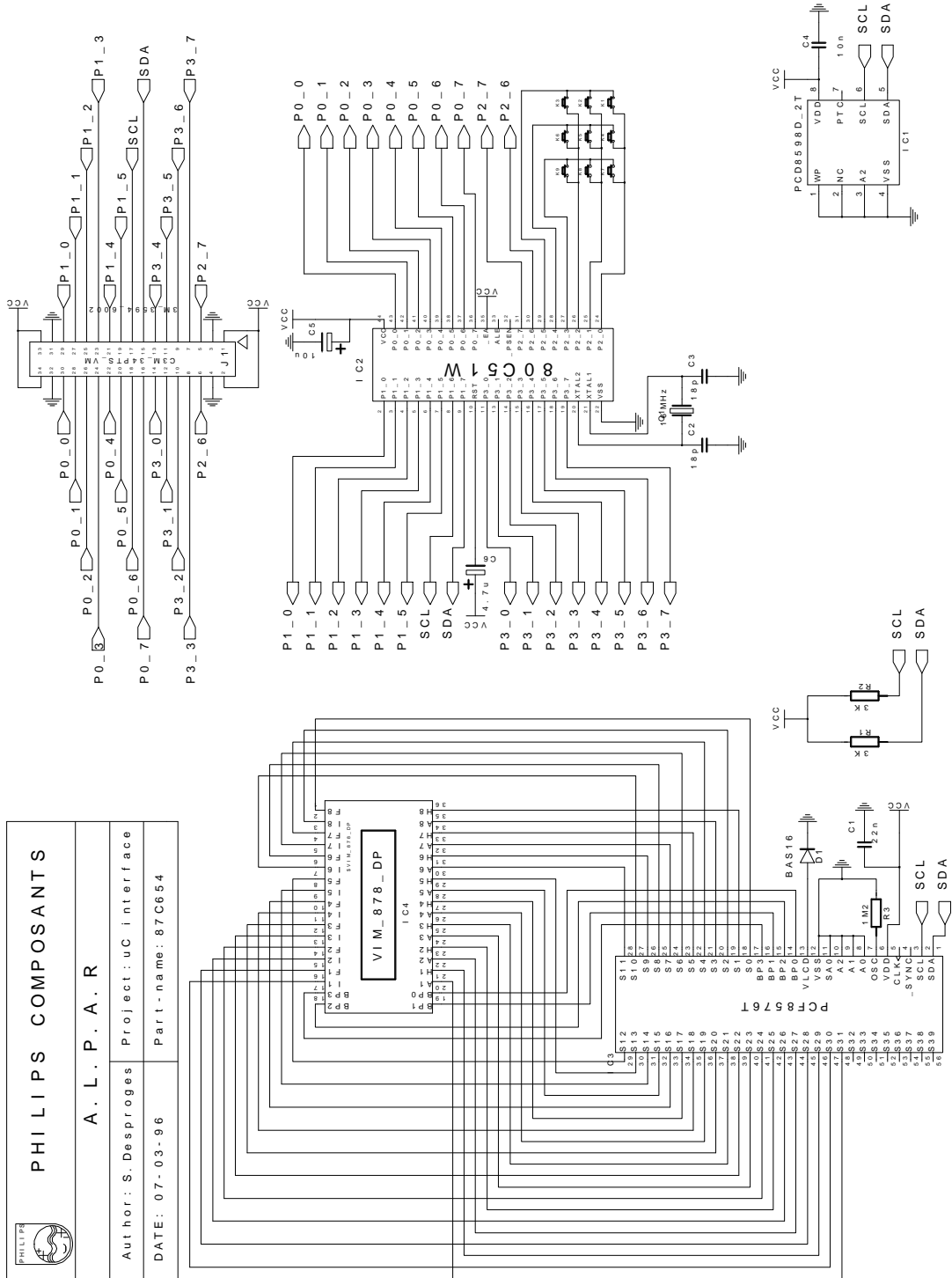
DEM08752-3 PCB-No: 514
EQUIPEMENT FACE SOUDURES

1.3 PART LIST

ANNEX 2

MICROCONTROLLER BOARD SCHEMATIC

**Triple high speed analog to digital converter
for LCD drive. TDA8752**



PHILIPS COMPOSANTS	
A. L. P. A. R.	
Author: S. Desproges	Project: uC interface
DATE: 07-03-96	Part - name: 87C654

ANNEX 3

MICROCONTROLLER SOFTWARE

DESCRIPTION OF THE SOFTWARE USED WITH THE MICROCONTROLLER BOARD INTERFACE

In order to program the TDA8752 for tests or for demonstrations, a software and an interface card are used. This software will be adaptable for a use with several ICs. The interface card is made of a keyboard of 9 buttons, a 8 digits LCD. This allows to display, to modify and to send the values to the different TDA8752 registers.

OBJECTIVES

Software function

This software allows the programming of the TDA8752 registers with a 9 buttons keyboard(see Fig.13).

The task must be simplified as much as possible for the user, so, the registers are organized in an unrolled menu as shown in the diagram in annex 2. At the power on sequence, it is possible to choose I²C or 3 wire bus transmission mode. The selection is done via the high and the low buttons, and the validation button (VAL).

The registers are organized in four menus :

- RED for the control registers of the RED analog signal.
- GREEN for the control registers of the GREEN analog signal.
- BLUE for the control registers of the BLUE analog signal.

The user chooses one of these menus, then the register with the help of the direction (high, low, right, left) and validation buttons.

The concerned register value is treated to be displayed.

The register modification is done digit by digit, with the help of the left and right buttons to move the cursor and of the complementation button to modify the concerned bit value.

At the validation, the modified value, will be stored.

If the 3 wire bus mode is selected, the data are transmitted to the TDA8752 automatically after the storage.

On the other hand, if the I²C bus is selected, the SEND button must be pressed to send the data. When all registers have been modified and not transmitted « SEND ALL » is displayed to give the possibility to send all data. This is done by pressing the SALL button. The fifth menu (named EEPROM) allows to save or read the data in the EEPROM. Thus, it is possible to save a configuration and to read it again from the EEPROM.

TDA8752 registers

Each of the 14 component registers has its own internal address, but without the same bits number. So, it is interesting to know the size (in bits and digits) of each register (cf. specification of the TDA8752).

The registers OFFSETx, COARSEx, and LINEx have the same size in the three menus RED, GREEN, and BLUE.

- OFFSETx: 8 digits coded on 8 BITS.
 - COARSEx: 7 digits coded on 7 BITS.
 - LINEx: 5 digits coded on 5 BITS.
- The clock menu registers are:
- CONTROL: 8 digits coded on 8 BITS.
 - VCO: 8 digits coded on 8 BITS.
 - DIVIDER: 8 digits coded on 8 BITS.
 - PHASEA: 6 digits coded on 6 BITS.
 - PHASEB: 6 digits coded on 6 BITS.

Every register has a byte allowed in RAM.

SOFTWARE ARCHITECTURE

Two transmission modes

The I²C wire

The I²C is a standard 2 wires serial communication interface (created by PHILIPS) using a defined protocol, which allows communication between several components. The SCL and SDA lines are respectively the clock wire and the data wire. They are unused at the high level.

Before the transmission begins, a memory zone is necessary in RAM to place the data which will be transmitted. The beginning address of this zone (75h) must be loaded in the MTD register.

The 3 wire bus

The 3 wire bus is constituted by :

- A clock wire (SCLOCK).
- A data wire (SDATA).
- A data validation wire (SEN).

The microcontroller has not specialized lines for the 3 wire bus. But the UART mode 0 can be used to generate the clock and data signals. The SCLOCK line becomes Txd (P3.1) and Rxd (P3.2) is used as SDATA line. One of the four I/O port is used for SEN (P3.6 has been chosen).

The common parts between the two transmission modes**Display of values and names**

The driver is controlled by I²C. Its slave address is 70h, it is configured by sending certain commands.

The MODE SET command allows the validation of the component and the configuration in « power saving » mode , « 1:4 mux » to activate the 4 lines BP, and so the 160 RAM bits will be used.

The LOAD DATA POINTER command corresponds to the internal RAM address on 8 bits. The bit 7 at logic « 0 » means that it is the last command, and bit 6 is fixed at logic « 0 » by the driver specification. The 6 LSB address bits of this command correspond to the organization described in annex 1.

The corresponding addresses of every digits are :

Address	DIGIT0	DIGIT1	DIGIT2	DIGIT3	DIGIT4	DIGIT5	DIGIT6	DIGIT7
Binary	000000	000100	001000	001100	010000	010100	011000	011100
Hexadecimal	00	04	08	0c	10	14	18	1c

After the digit number acquisition and during the register value display, this digit number is multiplied by 4, in order to have the digit address. Then it is placed in the I²C memory zone as a LOAD DATA POINTER command. To each digit corresponds a register REGDIG0 to REGDIG7 placed in the bit addressable memory (cf. registers list). These registers contain the displayed value of the corresponding digit.

Before display, the value must be transferred in the digit registers (REGDIGx). The value is in binary. These bits previously saved, are loaded in the bits 0 of the digits registers one after the other. Each number or letter is displayed by switching on segments, thanks to a 16 bits code.

The code numbers are in the TABVAL table classified in increasing order. To acquire these codes, the value to display (0 or 1) is multiplied by 2 (because there are 2 bytes per code; the result is placed in the accumulator A), then the first byte is read at the address A+#TABVAL and the second at the address (A+1)+#TABVAL.

The unused digits, that is to say the ones whose the number is inferior to the value of LIM (cf. registers list), of the concerned register are deleted by loading #0ah in their digit register (ex: the digits 0 and 1 of PHASEB). The value in TABVAL correspond to the code to delete all the digit segments. These codes are placed in I²C memory zone beginning with the digit 0 code (address 00h).

The loading in the driver is done by internal address auto incrementation.

Concerning the registers name, there is one display sub routine per name, with the same structure. After loading command and letters codes the data are sent. Letters are used more than once, so a subroutine was created per letter used.

Value modification

The subroutine MODIFREG allows the register value modification digit by digit. The selected digit is flanked by 2 points. During a left or right shifting, all the values are displayed one by one without point alight. Then the digits numbered POS and POS+1 are displayed with the point alight setting the DP bit at logic « 1 » (the bit 0 of 16 bits code). For the left digit (POS=0), only the digit 0 point is alight, switching off the digit 1 point and forcing POS to logic « 0 ».

For the right digit, POS is forced to 7, and it stays like this if the right button is still pressed. To modify the selected bit value, the complementation button (0/1) is pressed.

RAM storage

The RAM is not only used to display and modify the values (2.2.1.),but also for the storage. The bits 0 of the digits registers are placed one by one in the register RESb to be transferred at the address pointed by R0.

The EEPROM

Addressing the EEPROM

The bits 1 and 2 of the slave address of the EEPROM allow to choose the page which will be read or written. The possible addresses are:

MODE	PAGE1	PAGE2	PAGE3	PAGE4
READ	A1h	A3h	A5h	A7h
WRITE	A0h	A2h	A4h	A6h

The first transmitted byte is the wordaddress which is the internal address pointer from where data are read or written.

Data reading

Data which are stored in the EEPROM are the values of the TDA8752 registers from the address 00h of one of the pages. The WORDADDRESS must be initialized before every reading with the INITI routine which sends a 00h to the EEPROM. During the reading, the 14 registers are sent in the reserved register zone in RAM, charging the beginning address of this zone in the MRD register (cf. register list).

Data storage

The MEMEEPROM routine realizes this task. The storage in the EEPROM is done in « Page Write » mode. At each 8 bytes + WORDADDRESS sending, a 31,5 ms waiting time must be generated. A first loop (enc. label) allows to load, in the I²C memory zone, the data to transmit. The procedure, composed by the loops bcl1 and bcl2, allows the generation of the 31,5 ms waiting time. The « toujour » (cf. listing) allows to send the 16 bytes.

Note that only 14 bytes have to be stored, but in fact 16 bytes are stored to avoid the programming of a procedure to save the 8 first bytes and an other to save the 6 last.

The storage of the two supplementary "pseudo" registers is not important, because only 14 bytes are read in the reading routine.

Software heart

Two routines are used, one for the principal menu selection (named principal program), and the other for the registers and EEPROM menu (SELREGISTRE).

The principal program allows to move through the menu according to the button pressed. Only 3 buttons are used, high and low buttons for moving in the menu (6 is subtracted or added to the A contents), and VAL button for going to following level (3 is added to A).

SELREGISTRE function has the same structure as the principal program but left and right buttons are used to pass to the preceding level. The beginning address of a intermediate table is loaded in the DPTR, and an address Jump is generated (positive or negative adding or subtracting a value to the A contents) to move in this table.

Each address jump used, in the two different routines has for destination one of the « ljmp » instruction which constitutes the intermediate tables. Two of these « ljmp » are for the register or menu, which are constituted in two parts in the menu/register tables.

These tables are constituted by a serie of instructions which allow the generation of necessary actions for the registers management. Each register (or menu in the principal table) is divided in two parts :

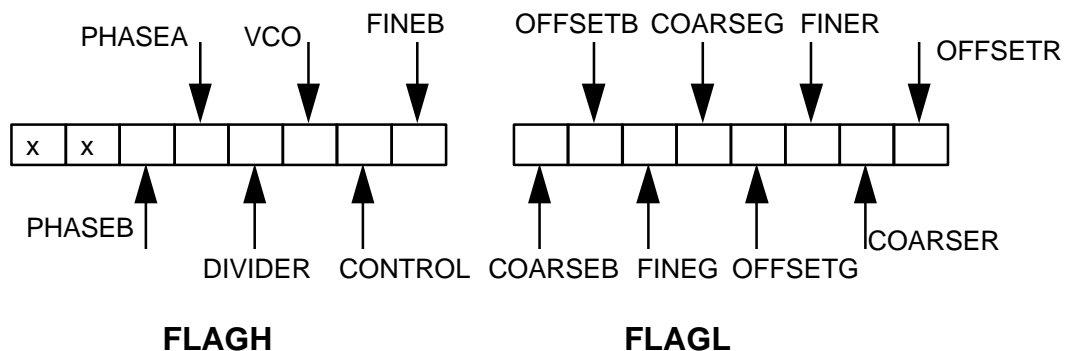
- The first (OFFSETR: for example), allows to display the register name during the shifting in the unrolled menu with high and low buttons.
- The second (OFFSETR2: for example) allows, when VAL button is pressed, to do all the operations concerning the selected register (display content, modify, memorize in RAM and send) or to pass to the following level in the principal table.

In many cases, the useful parameters used in some routines (like the register RAM address or his contents), are loaded in the accumulator A or in other registers (DPTR, R0, RESb...).

Transmission mode management

Transmission mode determination

The transmission mode is chosen at the power sequence. If the 3 wire bus is selected, the indicator bit « MODTRAN » is cleared; on the contrary, if the I²C bus is chosen, « MODTRAN » is set at « 1 ». The FLAGL and FLAGH registers are two 8 bits registers containing the 14 modification flag bits, indicating the modification of a register.



When a register was modified, that is when the complementation button was pressed at least once, the flag bit of the concerned register is set with the SETFLAG routine (cf. chart).

Pressing the SEND button, MODTRAN is tested, if the 3 wire bus was selected, no action is generated. Otherwise the value register, whose name is displayed, is sent by I²C and the flag bit is cleared. At this level the escape button allows to clear all the flags.

The ENVOI routine is called in the register table for each register. The « MODTRAN » bit is tested to determine if the data is automatically sent by 3 wire bus. Otherwise in I²C mode, the registers FLAGL and FLAGH are tested to know if all the registers are modified but not sent; in this case « SEND ALL » is displayed. When the SENDALL button is pressed, all the registers values are sent by I²C bus with the routine ENVTOUT and FLAGL and FLAGH are cleared.

In the other case ESCAPE must be pressed, any other buttons are usable.

Data transmission by 3 wire bus

The TDA8752 only receives data one by one in this mode. The word sent is a 8 bits data word, preceded by a 4 bits address. The transmission begins when the byte to send is loaded in the SBUF buffer, the bits are sent one by one from the LSB. So, the 12 bits word must be inverted in the following way.

The address of the value to send is pointed by R0 while the internal address is in RESh when the ENVTDA routine is called. Using the bit by bit rotation capability of the A accumulator, the 4 bits address are inverted and replaced in RESh, the data are inverted too. The result word is in RESh and A, therefore on 2 bytes. There are 4 bits unused, which must be sent first to be crushed by the following bits.

The word is as following :

A								R 0							
d0	d1	d2	d3	d4	d5	d6	d7	a0	a1	a2	a3	X	X	X	X

When a byte is sent, the bit TI must be set to 1, setting the UART control register(S0CON) to indicate that the serial port is free. After each byte sent, a ninth pulse is generated on the SCLOCK line.

The I²C bus data transmission to the TDA8752

Data are placed in I²C memory zone (from the RAM address 75h). In the case of data sending, the register internal address in RESh must be placed in the I²C zone, and after, the value of which the address is pointed by R0 is placed in the I²C zone too.

To send all the data, the value 1fh which is the TDA8752 mode 1 initial condition, and after the 14 data are placed in the I²C zone.

SOFTWARE EVOLUTION WITH TWO TDA8752

To manage two TDA8752, some modifications are necessary. Just after the choice of the transmission mode, it is possible to choose the management of one or two chips.

The CHOIX2 routine (cf. chart) sets the CHIP bit to one if there is one TDA8752 to manage. At the contrary, CHIP is cleared if there are two chips to manage. With one chip, the software is the same, than the first one. In the other case, each time that data must be sent (in 3 wire bus, I²C bus for one or all data), the chip, to which data will be transmitted, is chosen with the help of the CHOICHIP routine (cf. chart).

This routine allows the selection of the chosen component by loading the concerned chip slave address in SLA register and setting or clearing the SEN line, in 3 wire communication. For the 3 wire communication, the selection is done by the SEN line, which will be either set to 1 or to 0. In the case of two components, an inverter on the demo board allows the use of 1 SEN command (from the microcontroller). It will be then impossible to have both chips working at the same time.

ANNEX 4

I²C USER SOFTWARE

ANNEX 5

LCD SPECIFICATION